Remarks/Arguments

35 U.S.C. §112, ¶2

The Examiner has rejected claims 17-18, under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, Examiner has noted "it is not clearly understood how the second device is operative in said first mode of operation and a second mode of operation." (Office Action, page 3) The Examiner also noted that it was not clear how the "resistor is disconnected and connected to a power source during the same mode." (Office Action, page 3)

Claim 17 has been amended to describe that the first resistor is electrically isolated during the second mode of operation and electrically connected during the first mode of operation. Further, claim 17 has been amended to describe how the second subsystem can be operative in both the first and second modes of operation. Finally, claim 18 has been canceled.

In view of the above remarks and amendments to the claims, it is respectfully submitted that this rejection has been satisfied and should be withdrawn.

35 U.S.C. §102

Claims 5, 6, 11 and 12, stand rejected under 35 U.S.C. §102(b) as being anticipated by Schutte (U.S. Patent No. 5,689,196).

The present invention, as recited by currently amended claim 5, describes "an apparatus having a first mode of operation and a second mode of operation comprising: a data bus; a first power supply operating in said first mode, but not in said second mode; a second power supply operating in said first mode and said second mode; a transistor, responsive to a first power supply voltage level, with a base, collector and emitter wherein said first power supply is electrically coupled to base and collector, said data bus line being electrically coupled to the emitter, and said second power supply being electrically coupled to said data bus; wherein said transistor electrically isolates said data bus from said first

power supply in said second mode of operation and electrically connects said data bus to said first power supply in said first mode of operation."

It is respectfully asserted that Schutte fails to disclose a transistor which "electrically isolates said data bus from said first power supply in said second mode of operation and electrically connects said data bus to said first power supply in said first mode of operation," as described in currently amended claim 5.

Schutte teaches a system where "information is supplied to a bus in a wired logic function, the potential on the bus either being pulled down to ground level or remaining at supply level. The data line in a bus is split into two parts which are interconnected via the main current channel a transistor. Different supply voltages are used on the two parts. The control electrode of the transistor is connected to the lowest of the supply voltages. The transistor becomes conductive when either of the parts is pulled down. The transistor is non-conductive when none of the parts is pulled down." (Schutte Abstract)

The Office Action asserts that Schutte "teaches all claimed features in Fig. 1, an apparatus comprising a switch (16) responsive to a first power supply voltage level (V2) wherein said switch electrically isolates a data bus (20) from a second power supply (V1) in a first mode of operation (when the switch 16 is opened) and electrically connects said data bus to said second power supply in a second mode of operation (when the switch 16 is closed); wherein the switch is a transistor (16 is a transistor as seen)." (Office Action, pages 3-4)

Schutte discloses "a circuit in which data communication is possible between subcircuits incorporated in different integrated circuits operating with different supply voltages." (Col. 2, Lines 47-50) However, Schutte does not disclose an apparatus that can electrically isolate the data bus from a specific power supply, as described in the present invention. Instead, Schutte only discloses a method for keeping the circuit "suitable for data communication between the subcircuits." (Col. 5, Lines 46-47) In contrast, the present invention electrically isolates the specific power supply from the data bus by using the pull up voltage on the data bus which results in a reverse bias of the transistor that electrically

disconnects the data bus from the specific power supply. Thus, Schutte fails to disclose a transistor which "electrically isolates said data bus from said first power supply in said second mode of operation and electrically connects said data bus to said first power supply in said first mode of operation," as described in the current invention.

Claims 5-7, 11-15, and 17-24, stand rejected under 35 U.S.C. §102(b) as being anticipated by Greeff et al. (U.S. Patent No. 6,356,106).

The present invention, as recited by currently amended claim 5, describes "an apparatus having a first mode of operation and a second mode of operation comprising: a data bus; a first power supply operating in said first mode, but not in said second mode; a second power supply operating in said first mode and said second mode; a transistor, responsive to a first power supply voltage level, with a base, collector and emitter wherein said first power supply is electrically coupled to base and collector, said data bus line being electrically coupled to the emitter, and said second power supply being electrically coupled to said data bus; wherein said transistor electrically isolates said data bus from said first power supply in said second mode of operation and electrically connects said data bus to said first power supply in said first mode of operation."

It is respectfully asserted that Greeff also fails to disclose a transistor which "electrically isolates said data bus from said first power supply in said second mode of operation and electrically connects said data bus to said first power supply in said first mode of operation," as described in currently amended claim 5.

Greeff teaches a system where "an active termination circuit is incorporated into the devices connected to a multidrop bus. By including the active termination circuit on the devices instead of the bus, termination resistors can be removed from the system PCB, which saves costs and frees up precious space on the PCB. The active termination circuit has a termination enabled state and a termination disabled state. The active termination circuit is selectively placed into the enabled or disabled states in specified devices depending upon, for example, device location or communication traffic on the bus. The

multidrop system can also utilize a separate passive termination mechanism in combination with the active termination circuits utilized in the devices." (Greeff Abstract)

The Office Action asserts that Greeff "teaches all claimed features in Figs. 1 and 2, a television signal processing apparatus having a first device (11 Oa) operative in a first mode of operation (transmitting) and a second device (11 Ob) operative a second mode of operation (receiving) wherein said first device and said second device are both connected to at least one data bus line (102) wherein said data bus line is connected to a first power supply (VTERM) via a first resistor (124) integrated within said first device (11 Oa) and said data bus line is connected to a second power supply (VDD in Fig. 2) via a second resistor (224) integrated within said second device." (Office Action, page 4)

Greeff discloses "a termination scheme in a multidrop system that improves signal integrity on the system transmission line." (Col. 2, Lines 12-14) However, Greeff does not disclose any method for isolating a data bus from a specific power supply, as described in the present invention. Instead, Greeff only discloses that an "active termination circuit can be selectively programmed between a termination enabled state, where the circuit provides termination to the bus, and a termination disabled state, where the circuit does not provide termination to the bus." (Col. 4, Lines 42-46) In contrast, the present invention electrically isolates the specific power supply from the data bus by using the pull up voltage on the data bus which results in a reverse bias of the transistor that electrically disconnects the data bus from the specific power supply. Thus, Greeff fails to disclose a transistor which "electrically isolates said data bus from said first power supply in said second mode of operation and electrically connects said data bus to said first power supply in said first mode of operation," as described in currently amended claim 5.

In view of the above remarks and amendments to the claims, it is respectfully submitted that there is no 35 USC 112 enabling disclosure provided by Schutte or Greeff, alone or in combination, that makes the present invention as claimed in currently amended claim 5 unpatentable. It is further submitted that currently amended independent claims 11 and 17 are allowable for at least the same reasons that claim 5 is allowable. Since dependent claims 6-7, 12-15, and 18-24 are dependent from allowable independent claims 5, 11, and

17, it is submitted that they too are allowable for at least the same reasons that their respective independent claims are allowable. Thus, it is further respectfully submitted that this rejection has been satisfied and should be withdrawn.

35 U.S.C. §103

Claims 1-4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Greeff et al. in view of Jordan (U.S. Patent No. 5,336,948).

The present invention, as recited by currently amended claim 1, describes "an apparatus having a first mode of operation and a second mode of operation comprising: a data bus; a first power supply operating in said first mode, but not in said second mode; a second power supply operating in said first mode and said second mode; a third power supply operating in said first mode, but not in said second mode; and a transistor with a base, collector and emitter wherein said third power supply is electrically coupled to the base, said first power supply being electrically coupled to the collector, said data bus being electrically coupled to the emitter and said second power supply being electrically coupled to said data bus; wherein said transistor electrically isolates said data bus from said first power supply in said second mode of operation and electrically connects said data bus to said first power supply in said first mode of operation."

It is respectfully asserted that Greeff and Jordan, alone or in combination, fail to disclose a transistor which "electrically isolates said data bus from said first power supply in said second mode of operation and electrically connects said data bus to said first power supply in said first mode of operation," as described in currently amended claim 1.

Jordan teaches a system of "an active negation emulator circuit for improving the noise margin of signals carried by a signal interface bus. The circuit includes a sensor for sensing the voltage on the bus and a variable current source for supplying a current to the bus when the voltage level thereon is greater than a predetermined value. More particularly, when the voltage level on the bus is indicative of the signal carried thereby being in a logic high state, a current is supplied to raise the voltage level to the desired logic high voltage level. A combination circuit is also provided including an active negation emulator circuit, a resistive terminator, and switch means for selectively coupling the active negation

emulator to the signal interface bus, coupling the resistive terminator to the signal interface bus, or decoupling both the emulator and the terminator from the bus, in accordance with the location of the bus to which the combination circuit is coupled." (Jordan Abstract)

The Office Action asserts that Jordan "teaches the apparatus of claim 1 wherein the signal line (12) is connected to the emitter via a resistor (R3); wherein the resistor is located within a device (44); and wherein the device is an integrated circuit (44 constitutes an integrated circuit)." (Office Action, page 6)

Jordan discloses "an active negation emulator circuit operating as a responsive driver for improving the noise margin of logic signals carried by a signal interface bus, comprising a sensor for sensing the voltage on the bus, and a variable current source, coupled to the sensor, for supplying a current to the bus when the sensed voltage exceeds a first predetermined value." (Col. 1, Lines 53-59) However, Jordan does not disclose, nor did the Office Action assert that it discloses, an apparatus for isolating a data bus from a specific power supply, as described in the present invention. Instead, Jordan only discloses that when "the bus voltage exceeds the first predetermined value ... the variable current source supplies a current to the bus to raise the voltage level of the signal to the desired logic high voltage amplitude. Furthermore, the supply of current is stopped when the bus voltage exceeds the second predetermined value ... this way, excess power dissipation caused by unnecessary supplying current ... is prevented." (Col. 2, Lines 7-19) In contrast, the present invention electrically isolates the specific power supply from the data bus by using the pull up voltage on the data bus which results in a reverse bias of the transistor that electrically disconnects the data bus from the specific power supply. Thus, Jordan, like Greeff, fails to disclose a transistor which "electrically isolates said data bus from said first power supply in said second mode of operation and electrically connects said data bus to said first power supply in said first mode of operation," as described in currently amended claim 1.

In view of the above remarks and amendments to the claims, it is respectfully submitted that there is no 35 USC 112 enabling disclosure provided by Greeff or Jordan, alone or in combination, that makes the present invention as claimed in currently amended

claim 1 unpatentable. Since dependent claims 2-4 are dependent from allowable independent claim 1, it is submitted that they too are allowable for at least the same reasons that claim 1 is allowable. Thus, it is further respectfully submitted that this rejection has been satisfied and should be withdrawn.

In the Drawings

The Examiner has objected to the drawings under 37 C.F.R. 1.83(a). Specifically, Examiner stated that "the plurality of switches and the plurality of bus lines must be shown or the feature(s) cancelled from claims 10 and 16."

Claims 10 and 16, which contained the language referenced by the Examiner, have been canceled. Thus, it is respectfully submitted that the rejection has been satisfied and should be withdrawn.

Having fully addressed the Examiner's rejections it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's representative at (609) 734-6804, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,

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